In the Claims

Amend the claims as follows:

1. (Previously Amended) A memory system comprising:

a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals;

a register programmed to provide inverted and non-inverted signals to the DRAMs; and

programmable pins in the register and the DRAMs to enable operation in either non-inverted or inverted mode, wherein a first programmable pin is connected to ground to enable an inverting mode and a second programmable pin is connected to Vdd to operate in a non-inverting mode.

2. (Previously Amended) The memory system of claim 1 which indicates re-drive circuitry, which can output both non-inverted and inverted polarity signals from one or more input signals.

3. (Canceled)

4. (Previously Amended) The memory system of claim 1 wherein the DRAMs are mounted on a DIMM.

5. (Canceled)

6. (Previously Amended) A memory system comprising:

a plurality of DRAMs having receiver circuits adapted to interface with a plurality of signal drivers capable of providing both non-inverted and inverted address and command signal polarities to the plurality of DRAMs; and

a memory controller capable of enabling the plurality of DRAMs to accept either non-inverted or inverted signals using the programmable pin, which dynamically configures the polarities of address and command signals exchanged between a plurality of signal drivers and

the plurality of DRAMs, such that simultaneous switching noise in the memory system is reduced.

7. (Canceled)

8. (Original) The memory system of claim 6 wherein the pin is hardwired to the DRAMs.

9. (Original) A memory system of claim 1 in which the register drives either non-inverted or inverted signals to the DRAMs using a programmable pin.

10. (Previously Amended) A memory system comprising:

a module having a plurality of DRAMs with inputs and outputs and circuits to accept either non-inverted input signals or inverted input signals, wherein pre-selected DRAMs may operate in inverted mode with some critical signals remaining in a non-inverted mode;

a means connected to the circuit for changing modes to accept inverted input signals; and

a memory controller which is programmable to operate in non-inverted mode at power up and to change after it is programmed.

11. (Canceled)

12. (Original) The memory system of claim 10 wherein the memory controller may operate in the inverted mode with some critical signals remaining in the non-inverted mode.

13. (Original) The memory system of claim 10 wherein a programmable pin is hard-wired to the module.

14. (Original) The memory system of claim 10 wherein the means for changing modes includes a pin that is controlled by the memory controller.

15-17. (Canceled)